Remarks

The above Amendments and these Remarks are in reply to the outstanding Office action. Claims 1-3, 5-8, 10-26 and 28-33 are presented herewith for consideration. Claim 11 has been amended to correct a typographical error. Claim 25 has been amended.

Claims 1-3, 5-8 and 12-24 are allowed.

Claim 11 is objected to because of containing informalities. As suggested by the Examiner, claim 11 has been amended and it is therefore respectfully requested that the objection be withdrawn.

Claim 25 is rejected under 35 U.S.C. §102(e) as being anticipated by *Chiu* (U.S. Patent No. 6,642,747).

Claims 26 and 27 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Chiu* in view of *Shastri* (U.S. Publication No. 2002/0105386 A1).

Claim 28 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Chiu* in view of *AOAPA* (applicants' own admitted prior art).

Claims 29-33 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Beherns* (U.S. Patent No. 5,572,558) in view of *Chiu.*

I. Rejection of Claim 25 under 35 U.S.C. §102(e)

Claim 25 is rejected under 35 U.S.C. §102(e) as being anticipated by *Chiu* (U.S. Patent No. 6,642,747).

Claim 25 has been amended to include the limitations of claim 27 and therefore is at least patentable for the reasons stated below.

In rejecting claims 25 under 35 U.S.C. §102(e) the Office Action stated:

> Chiu discloses…the clock circuit comprises, an averaging circuit … (Fig. 4. Phase detector 410 is arranged to produce a first up and down signal (UP1, DOWN1) in response to comparing the phases between a reference clock signal (REF_CLK) and a VCO output clock signal (VCO_CLK). Over a given time interval, the average value the of UP1 and DOWN1 signals will correspond to the phase difference between the VCO_CLK signal and the REF_CLK signal. The phase-detector is thus employed to adjust the phase relationship between the VCO clock signal and the reference clock signal. Office Action, page 3.

In contrast to *Chiu*, amended claim 25 calls for **both** "a phase detector to output a plurality of up signals and a plurality of down signals in response to the data signal; [and] a clock circuit … [that] comprises, an averaging circuit…" (Emphasis added.) Chiu discloses "phase detector 410," but not "a clock circuit … [that]comprises, an averaging circuit capable to output the phase adjust signal in response to an average up signal, obtained from the plurality of up

signals in a predetermined period of time, and an average down signal, obtained from the plurality of down signals in the predetermined period of time."

It is therefore respectfully requested that the rejection of claim 25 be withdrawn.

II. Rejection of Claims 26 and 27 under 35 U.S.C. §103(a)

Claims 26 and 27 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Chiu* in view of *Shastri* (U.S. Publication No. 2002/0105386 A1).

Claims 26 and 27 depend from claim 25 and therefore are patentable for at least the reasons stated above in regard to claim 25.

It is therefore respectfully requested that the rejection of claims 26 and 27 be withdrawn.

III. Rejection of Claim 28 under 35 U.S.C. §103(a)

Claim 28 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Chiu* in view of *AOAPA* (applicants' own admitted prior art).

Claim 28 depends from claim 25 and therefore is patentable for at least the reasons stated above in regard to claim 25.

It is therefore respectfully requested that the rejection of claim 28 be withdrawn.

IV. Rejection of Claims 29-33 under 35 U.S.C. §103(a)

Claims 29-33 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Beherns* (U.S. Patent No. 5,572,558) in view of *Chiu.*

In rejecting independent claims 29, 30 and 33, the Office Action repeatedly states:

> Beherns discloses all the limitations claimed but fails to explicitly disclose whether the PLL consists of an averaging circuit/method…however Chui discloses a PLL system …comprising an averaging circuit…
>
> Thus, it would have been obvious to a person of ordinary skill in the art to use the averaging circuit disclosed by Chui because it [sic] the UP and DOWN signals in the circuit allow the PLL to adjust phase and frequency of the VCO. (Emphasis added.) Office Action, pages 8-14.

The Applicant's attorney respectfully disagrees. *Beherns* **already** discloses a PLL that adjusts phase (see "phase error detector F54") and frequency (see "frequency error detector F52") of a "variable frequency oscillator F50". Furthermore, *Chui* discloses clock signals "REF_CLK and VCO_CLK" input to "phase detector 410." In contrast, *Beherns* discloses data signals "expected sample values x(n) F58" and "estimated sample values X(n)F60" input to "a phase error detector F54" that outputs "phase error F123."

Claims 31 and 32 depend from claim 30 and therefore are patentable for at least the reasons stated above in regard to claim 30.

It is therefore respectfully requested that the rejection of claims 29-33 be withdrawn.

V. Conclusion

Based on the above amendments and these remarks, reconsideration of claims 1-3, 5-8, 10-26 and 28-33 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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